AMENDMENTS TO THE SPECIFICATION

Page 25, lines 1 - 5

NAND flash memory cell array and fabrication process in which control gates and floating gates are stacked in pairs arranged in rows between a bit line diffusion and a common source diffusion, with select gates on both sides of each of the pairs of stacked gates. The gates in each stacked pair are self-aligned with each other and with the select gates adjacent to them. In one disclosed embodiment, the select gate at one end of each row partially overlaps the common source diffusion, and in another it lies directly above the source diffusion and is common to groups of cells on both sides of the diffusion.